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P. Walker
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XA-9472

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yasuhisa SHIMAZAKI et al.

Appln. No.: 09/855,660 Group Art Unit: 2811

Filed: May 16, 2001

For: SEMICONDUCTOR INTEGRATED CIRCUIT

SUPPLEMENTAL PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Supplementing the Preliminary Amendment filed May 16, 2001, please further amend the above-identified patent application as indicated below.

IN THE SPECIFICATION:

Please delete the paragraph beginning at page 2, line 8 and replace it with the following replacement paragraph:

B1

To address the request for reduction in power consumption, Japanese Unexamined Patent Publication No. Hei 10(1998)-189749 (U.S. Patent No. 6,097,043) (second literature) discloses a method of preparing a plurality of power supply voltages and selectively using a circuit for supplying a high voltage and a circuit for supplying a low voltage, thereby reducing the power.